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IN THE CLAIMS:

Amendments to the Claims

Please amend the claims as shown below.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (original) A method for structuring a planar substrate composed of a glasslike material,

characterized by a combination of the following method steps:

- provision of a semiconductor planar substrate composed of a semiconductor material,
- reduction of the thickness of said semiconductor planar substrate inside at least one surface region of said semiconductor planar substrate in order to form a raised surface region in relation to said surface planar region of reduced thickness,
- structuring said raised surface region of said semiconductor planar substrate by means of local mechanical removal of material in order to place impressions inside said raised surface regions,
- joining said structured surface of said semiconductor planar substrate with said glasslike planar substrate in such a manner that said glasslike planar substrate at least partially covers said surface planar region of reduced thickness,
- tempering said joined planar substrates in such a manner that in a first tempering phase, which is conducted under vacuum conditions, said glasslike planar substrate covering said surface region of reduced thickness forms a fluid-tight bond with said surface region of reduced thickness, with said planar substrate covering said impressions in a fluid-tight manner under vacuum conditions, and that in a

second tempering phase, at least partial areas of the glasslike material flow into said impressions of said structured surface of said semiconductor planar substrate.

2. (original) A method for structuring a planar substrate composed of a glasslike material,

characterized by a combination of the following methods steps:

- provision of a semiconductor planar substrate composed of a semiconductor material,
- reduction of the thickness of said semiconductor planar substrate inside at least one surface region of said semiconductor planar substrate in order to form a raised surface region in relation to said surface region of reduced thickness,
- structuring of said raised surface region of said semiconductor planar substrate by means of local mechanical removal of material in order to place impressions inside said raised surface region,
- structurally conform deposition of a metal layer onto said structured, raised surface region,
- joining said structured, metallized surface with said glasslike planar substrate in such a manner that said glasslike planar substrate at least partially covers said surface region of reduced thickness,
- tempering said joined planar substrates in such a manner that in a first tempering phase, which is conducted under vacuum conditions, said glasslike planar substrate covering said surface region of reduced thickness forms a fluid-tight bond with said surface region of reduced thickness, with said planar substrate covering said impressions under vacuum conditions in a fluid-tight manner, and that in a second tempering phase, at least partial areas of said glasslike material flow into said impressions of said structured, metallized surface of said semiconductor planar substrate.

3. (currently amended) The method according to claim 1~~-or 2~~,

wherein said reduction in thickness is carried out at the edge region of said semiconductor planar substrate.

4. (original) The method according to claim 3,

wherein said reduction in thickness is carried out in such a manner that said raised surface region is limited by a boundary area and is at least partially surrounded by said edge region of reduced thickness.

5. (currently amended) The method according to claim 3~~-or 4~~,

wherein said reduction in thickness is conducted by means of a wet-chemical etching process or a mechanical material processing method.

6. (currently amended) The method according to ~~one of the claims~~ <u>claim</u> 1 ~~to 5~~,

wherein said structuring of said raised surface region of said semiconductor planar substrate occurs by means of local mechanical removal of material in such a manner that impressions, which have a structural depth extending maximally to the plane of said surface region of reduced thickness, are worked inside said raised surface region by means of a removal tool.

7. (currently amended) The method according to ~~one of the claims~~ <u>claim</u> 1 ~~to 6~~,

wherein a sawing, abrading or milling tool is employed as said removal tool.

8. (currently amended) The method according to claim 6~~-or 7~~,

wherein said removal tool is moved in relation to said semiconductor planar substrate in such a manner that for selective removal of material, said removal tool is moved laterally over the surface of said surface region of reduced thickness in said raised surface region.

9. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 8~~,

wherein said removal of material results in straight or curved running impressed channels within said raised surface region.

10. (original) The method according to claim 9,

wherein said impressed channels are open toward the surface of said raised surface region and project open through the lateral boundary wall of said raised surface region.

11. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 10~~,

wherein joining said semiconductor planar substrate with said structured planar substrate occurs by means of anodic bonding or thermal bonding.

12. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 11~~,

wherein during said second tempering phase, normal pressure conditions or high pressure conditions prevail, which act on the surface of said glasslike planar substrate facing away from said semiconductor planar substrate.

13. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 12~~,

wherein said tempering is carried out by controlling the temperature and the duration in such a manner that said glasslike material stops flowing into said impressions in said semiconductor planar substrate when said glasslike material completely fills said impressions.

14. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 13~~,

wherein following said tempering, two-dimensional removal of material is carried out in such a manner that said glasslike planar substrate assumes a flush adjoining surface to said structured surface of said semiconductor planar substrate.

15. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 14~~,

wherein semiconductor material is removed from the surface of said semiconductor planar substrate facing the surface joined with said glasslike planar substrate until at least partial areas of said glasslike material which flowed into said impressions are uncovered, said partial areas being flush with said surface of said semiconductor planar substrate.

16. (currently amended) The method according to ~~one of the claims~~ claim 1~~, 3 to 15~~,

wherein said semiconductor material is separated from said glasslike planar substrate.

17. (original) The method according claim 16,

wherein said separation of said glasslike planar substrate from said semiconductor planar substrate occurs by means of etching away said semiconductor material.

18. (original) The method according to claim 16,

wherein said separation of said two planar substrates occurs by providing a separation layer between said two planar substrates.

19. (original) The method according to claim 18,

wherein said separation layer is applied onto said structured surface of said semiconductor planar substrate before joining said two planar substrates in a structure-retaining manner and is designed as a sacrificial layer which is destroyed by means of thermal and/or chemical action and permits separating said two substrates.

20. (currently amended) The method according to claim 18~~ or 19~~,

wherein a metal layer which has a melting point which lies below the melting points of said substrates is utilized as said separation layer.

21. (currently amended) The method according to claim 18~~ or 19~~,

wherein a layer capable of oxidizing which changes chemically under the addition of oxygen and/or thermal energy is utilized as said separation layer.

22. (currently amended) The method according to claim 18~~ or 19~~,

wherein a carbon layer, diamond layer, diamond-like layer or SiC is utilized as said separation layer.

23. (currently amended) The method according to ~~one of claims~~ claim 16 ~~to 22~~,

wherein after separation of said two planar substrates from each other, said glasslike planar substrate is finished mechanically in order to retain said perforations penetrating perpendicularly through said planar substrate.

24. (original) The method according to claim 23,

wherein said perforations are filled with an electrically conductive material.

25. (currently amended) The method according to ~~one of the claims~~ claim 2 ~~to 15~~,

wherein before structurally conform deposition of said metal layer on said structured raised surface region, a protective layer is deposited on said semiconductor planar substrate in order to prevent reactions between said semiconductor planar substrate and said metal layer.

26. (currently amended) The method according to ~~one of the claims~~ claim 2 ~~to 15 or 25~~,

wherein before joining said structured, metallized surface with said glasslike planar substrate, at least partial areas of said metallized surface are removed.

27. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 26~~,

wherein said glasslike material and said semiconductor material posses almost the same thermal expansion coefficients.

28. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 27~~,

wherein said planar substrate composed of a glasslike material is a borosilicate glass.

29. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 28~~,

wherein said semiconductor planar substrate is a silicon substrate.

30. (currently amended) The method according to claim 25 ~~and 29~~,

wherein thermal SiO_2 is deposited as said protective layer.

31. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 30~~,

wherein said structuring of said semiconductor planar substrate results in impressions of structural dimensions in the micrometer and/or sub-micrometer range.

32. (currently amended) The method according to ~~one of the claims~~ claim 1 ~~to 31~~,

wherein said impressions have an aspect ratio (height, respectively depth: width) of 10:1.

33. (currently amended) A glasslike planar substrate produced according to ~~one of~~ the ~~methods~~ method according to ~~claims~~ claim 1 ~~to 32~~,

wherein said glasslike planar substrate is penetrated perpendicular to the substrate surface by perforations in which electrically conductive material is provided.

34. (original) The glasslike planar substrate according to claim 33,

wherein said perforations filled with electrically conductive material are arranged arraylike.

35. (currently amended) Use of said glasslike planar substrate according to claim 33 ~~or claim 34~~ for electrical contacting of components in microelectronics or micromechanics.

36. (currently amended) The use of said method according to ~~claims~~ claim 1 ~~to 15 or 25 to 32~~ for producing a semiconductor planar substrate penetrated by a glasslike material.

37. (original) A semiconductor planar substrate produced according to claim 36,

wherein said semiconductor planar substrate is a silicon wafer which, for the purpose of electrical and/or thermal insulation or for reasons of optical transparency, is provided with areas of glasslike material at least partly penetrating said silicon wafer.

38. (currently amended) The semiconductor planar substrate according to claim 36 ~~or claim 37~~,

wherein said areas of glasslike material which at least partly penetrate said silicon wafer enclose at least one semiconductor region, and

wherein a metal layer is provided at least between said enclosed semiconductor region and said areas of glasslike material.

39. (original) The semiconductor planar substrate according to claim 38, **wherein** said enclosed semiconductor region is covered on both sides with an electrode structure respectively, each of which contacting said metal layer enclosing said semiconductor region.